

CLAIMS

What is claimed is:

- 1 1. In a data processing system including a cache memory and a system memory
2 coupled to a processor, a method for executing a computer program, comprising, in
3 response to executing an instruction that references data in the system memory and that
4 specifies an alternate control path:
5 determining whether the data referenced in the instruction are present in the cache
6 memory; and
7 changing control flow of the program in accordance with the specified alternate
8 control path if the referenced data are not present in the cache memory.
- 1 2. The method of claim 1, further comprising:
2 returning the data referenced in the instruction from the cache memory to the
3 processor if the referenced data are present in the cache memory; and
4 returning the data referenced in the instruction from the system memory to the
5 processor if the referenced data are not present in the cache memory.
- 1 3. The method of claim 2, wherein changing control flow further comprises
2 branching to a program address specified by the instruction.
- 1 4. The method of claim 2, wherein changing control flow further comprises skipping
2 an instruction.

1 5. The method of claim 1, further comprising returning the data referenced in the
2 instruction from the cache memory to the processor only if the referenced data are present
3 in the cache memory.

1 6. The method of claim 5, further comprising, if the referenced data are not present in
2 the cache memory, loading the data referenced in the instruction from the system memory
3 to the cache memory.

1 7. The method of claim 5, further comprising if the referenced data are not present in
2 the cache memory, bypassing loading of the data referenced in the instruction from the
3 system memory to the cache memory.

1 8. The method of claim 5, wherein changing control flow further comprises
2 branching to a program address specified by the instruction.

1 9. The method of claim 5, wherein changing control flow further comprises skipping
2 an instruction.

1 10. The method of claim 1, further comprising:
2 if the data are present in the cache memory, bypassing loading of the referenced
3 data from the cache memory to the processor;
4 if the data are not present in the cache memory, bypassing loading of the
5 referenced data from the system memory to the cache memory.

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- 1 11. The method of claim 10, wherein changing control flow further comprises
2 branching to a program address specified by the instruction.
- 1 12. The method of claim 10, wherein changing control flow further comprises skipping
2 an instruction.
- 1 13. The method of claim 1, wherein changing control flow further comprises
2 branching to a program address specified by the instruction.
- 1 14. The method of claim 1, wherein changing control flow further comprises skipping
2 an instruction.
- 1 15. A computing arrangement comprising:
2 a processor configured to execute a program;
3 a cache memory coupled to the processor;
4 a system memory coupled to the cache memory, wherein the processor is
5 configured to execute an instruction that references data in the system memory and that
6 specifies an alternate control path in the program;
7 means for determining whether the data referenced in the instruction are present in
8 the cache memory; and
9 means for changing control flow of the program in accordance with the specified
10 alternate control path if the referenced data are not present in the cache memory.